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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/089,192	03/27/2002	Haruyoshi Toyoda	112417	5206

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EXAMINER	
LAM, HUNG H	

ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 08/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/089,192	TOYODA ET AL.	
	Examiner	Art Unit	
	Hung H. Lam	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Election/Restrictions

2. Applicant timely traversed the restriction (election) requirement in the reply filed on 07/08/05. In view of Applicant's arguments, the election of species requirement is hereby withdrawn. Therefore, claims 1-12 are now considered on the merits.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3 and 5-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda (US-6,115,066) in view of Blessinger (US-5,196,938).

It is noted that the USPTO considers the Applicant's "one of" language to be anticipated by any reference containing one of the subsequent corresponding elements.

With regarding to **claim 1**, Gowda discloses a camera for high-speed image processing, comprising:

photodetector array having plurality photodetectors (Fig. 3; pixels 30), which are arranged two-dimensionally plurality rows and plurality columns and which are divided into a plurality blocks (Fig. 3; Col. 2, Ln. 65-67 – Col. 3, Ln. 1-11; Col. 4, Ln. 42-58; a plurality of blocks is interpreted as a plurality of column of pixels wherein each column of pixels is connected to the respective column bus 15_1-15_N), the photodetector array repeatedly receiving optical images and generating output signals for the optical images in a plurality of consecutive frames at a predetermined frame rate (Fig. 3; Col. 6, Ln. 35-36; Col. 7, Ln. 18-21; the plurality of pixels 30 inherently receive optical images and generate output signals. The output signals are inherently formed a plurality of consecutive frames at a predetermined frame rate. Gowda further teaches that the column select/ scan logic 44 outputs the final image data 43 to the image storage and processing electronic);

an analog-to-digital converter array (Fig. 3; A/D converters 40_1-40_N) including plurality of analog-to-digital converters correspondence with the plurality one-on-one blocks the photodetector array (see the arrangement of the rows/ columns of pixels in Fig. 3), each analog-

to-digital converter performing analog-to-digital conversion of the output signals which are read sequentially from the photodetectors in the corresponding block (Col. 3, Ln. 1-15; Col. 4, Ln. 7-30; Figs. 3 and 4 show the A/D $\{40_1$-$40_N\}$ connecting to the columns of the array of pixels 30 respectively. It is inherent that the A/D converter must sequentially perform the conversion for each of the pixels signal in the corresponding column);

an image-processing unit performing predetermined parallel processes on digital signals (Col. 3, Ln. 15-20; Col. 7, Ln. 3-21; the digital signals are processed with the double correlated sampling operation), which are transferred from the analog-to-digital converter array and which correspond to the signal outputted from the photodetectors, thereby generating a processed result signal indicating results of the processes (Col. 3, Ln. 21-26; Col. 7, Ln. 3-20; Gowda teaches that each column of pixels 30 is connected to the corresponding A/D converter and the register 40_1-40_N for processing noise removal);

Gowda teaches a signal converter (Fig. 3; 44) that has at least one of the processed result signal and the output signal from the analog-to-digital converter array to be inputted and thereby outputting an image signal (Col. 6, Ln. 30-36; Col. 7, Ln. 18-21; Gowda teaches that the column select/ scan logic 44 outputs the final image data 43 to the image storage and processing electronic in accordance to the noise removal operation and the outputted signal from the A/D converter).

However, Gowda fails to disclose:

a selector selecting at least one frame based on processed results obtained by the image-processing unit;

a signal converter converting, into an image signal of a desired frame rate, and

a signal conversion controller controlling the signal converter to perform the image signal conversion operation for the at least one frame selected by the selector. However, the limitations are well known in the art as taught by Blessinger.

In the same field of endeavor, Blessinger teaches a camera comprising a selector/multiplexer (Fig. 2; 22), which is used to produce image frame signal (Fig. 2; multiplexer 22; Col. 3, Ln. 40-44). Blessinger further teaches an additional selector/ multiplexer (Fig. 1; 28) for selectively associating the external data with the image frame signal from the A/D converter (Col. 3, Ln. 65-67). Additionally, Blessinger teaches a signal converter (Fig. 1; 30, 34, and 36) wherein a central controller (Fig. 1; 36) controls the image memory (Fig. 1; 30) and processor (Fig. 1; 34) to adjust the frame rates of the playback frame on the display monitor (Fig. 1; 32) (Figs. 1-2; Col. 4, Ln. 32-40). In light of the teaching from Blessinger, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a selector and a signal conversion circuit as taught by Blessinger in the device of Gowda in order to provide an improved camera which records an event at fast frame rate and plays back the event at a slow frame rate (Col. 1, Ln. 6-13).

With regarding to **claim 2,** Gowda in view of Blessinger discloses a camera for high-speed image processing wherein the desired frame rate is lower than the predetermined frame rate (Blessinger; Col. 1, Ln. 7-17; Blessinger teaches a camera which records an event at a fast frame rate and plays back the event at a slower frame rate so that the event may be analyzed; therefore, it is inherent that the desired play-back frame rate is slower than the predetermined frame rate/ recording frame rate).

With regarding to **claim 3**, Gowda in view of Blessinger discloses a camera for high-speed image processing wherein the signal converter (Blessinger; Fig. 1, 30, 34, 36) converts the output signal from the analog-to-digital array (Blessinger; Fig. 1; ADC 26) and processed result signals into the image signal of the desired frame rate, and outputs the image signal (Blessinger; Col. 4, Ln. 32-40).

With regarding to **claim 5,** Gowda in view of Blessinger discloses a camera for high-speed image processing wherein the signal converter has a buffer memory (Blessinger; Fig. 1; 30) at a signal input side thereof, the buffer memory storing at least one of the output signal from the analog-to-digital converter array (Blessinger; Fig. 1; ADC 26) for at least several frames and the processed result signal for at least several frames (Blessinger; Col. 4, Ln. 3-31; Col. 4, Ln. 45-62).

With regarding to **claim 6,** Gowda in view of Blessinger discloses a camera for high-speed image processing further comprising a data buffer storing predetermined process data (Gowda; Col. 3, Ln. 15-21; Col. 7, Ln. 3-16; registers 42_1-42_N and 44 are interpreted as the data buffer; the predetermined process data are interpreted as the first and second codewords), the image-processing unit performing predetermined parallel process, using the predetermined process data (Gowda; Col. 7, Ln. 15-20; because of the arrangement of the registers 42_1-42_N and 44 in Fig. 3, the image-processing unit performs a parallel subtraction between signals corresponding to the first and second codewords), onto digital signals that are transferred from

the analog-to-digital converter array and that correspond the signals outputted from photodetectors (Gowda; see Fig. 3; Col. 3, Ln. 53-67; Col. 7, Ln. 1-15).

With regarding to **claims 7 and 8,** Gowda in view of Blessinger discloses a camera for high-speed image processing wherein the plurality analog-to-digital converters in the analog-to-digital converter array (Gowda; Fig. 3; A/D converters 40_1-40_N) are provided one-on-one correspondence with the plurality of rows/columns of photodetectors (Gowda; Fig. 1; rows/columns of array of pixels 30) in the photodetector array (Gowda; Col. 3, Ln. 53-67; see the arrangement of array of pixels 30 and A/D converters 40_1-40_N in Fig. 3).

With regarding to **claim 9,** Gowda in view of Blessinger discloses a camera for high-speed image processing wherein the image-processing unit includes a plurality processors one-to-one correspondence with the plurality of photodetectors (Gowda; Col. 3, Ln. 54-7 – Col. 4, Ln. 1; registers 42_1-42_N and 44 corresponding to the rows/columns of array of pixels 30 are interpreted as the processors which are used to process the first and second codewords), the plurality of procesors (Gowda; Fig. 3; registers 42_1-42_N and 44) performing parallel processes on the digital signals that are transferred from the analog-to-digital converter array and that correspond to the signals outputted from the plurality of photodetectors (Gowda; Col. 3, Ln. 15-21; Col. 7, Ln. 1-20; see the arrangements of processor/ registers 44, 42_1-42_N , A/D converter 40_1-40_N, and array of pixesls 30).

With regarding to **claim 10,** Gowda in view of Blessinger discloses a camera for high-speed image processing wherein the image-processing unit (Gowda; Fig. 3; 42_1-42_N) includes least one parallel processing circuit (Gowda; Fig. 3; registers 42_1-42_N and 44 are interpreted as the image-processing unit), each of the at least one parallel processing circuit performing a corresponding parallel process on the digital signals that are transferred from the analog-to-digital converter array and that correspond the signals outputted from photodetectors (Gowda; Col. 3, Ln. 53-67), thereby outputting a processed result signal indicative of the processed result (Gowda; Col. 3, Ln. 67- Col. 4, Ln. 4; the double correlated sampling operation results in noise removal), the selector (Blessinger; Figs. 1-2; multiplexers 22 and 28) selecting at least one frame based on at least one process result from the at least one parallel processing circuit (Blessinger; Col. 3, Ln. 40-43; Col. 3, Ln. 65-67; Blessinger teaches that the selector/multiplexer 22 produces image frame signal), the signal converter (Blessinger; Fig. 1; 30, 34, 36) converting at least one of the output signal from the analog-to-digital converter array and the processed result signal obtained by the at least one parallel processing circuit (Blessinger; Col. 4, Ln. 33-40; Blessinger teaches a converter for varying the outputted frame rate from the A/D converter), into the image signal of the desired frame rate, and outputting the image signal (Blessinger; Col. 4, Ln. 33-40; Blessinger teaches a converter for varying the outputted frame rate).

With regarding to **claim 11,** Gowda in view of Blessinger discloses a camera for high-speed image processing wherein each of the at least one parallel processing circuit (Gowda; Fig. 3; registers 42_1-42_N) are provided with several processing elements in one-to-one correspondence

with several blocks that make up at least a portion of all the plurality of blocks in the photodetector array (Gowda; see the arrangement of register 42, and the rows/columns of array of pixels 30 in Fig. 3), each of the several processing elements performing a predetermined parallel process on the digital signals that are transferred from the corresponding analog-to-digital converter and that are equivalent to the signals outputted from photodetectors existing in the corresponding block (Gowda; Col. 3, Ln. 12-21; Col. 3, Ln. 53-67).

With regarding to **claim 12,** Gowda in view of Blessinger discloses a camera for high-speed image processing wherein plurality analog-to-digital converters the analog-to-digital converter array (Gowda; Fig. 3; A/D 40_1-40_N) are provided one-to-one correspondence with the plurality rows photodetectors the photodetector array (Gowda; see the arrangement in Fig. 3), each of the at least one parallel processing circuits (Gowda; Fig. 3; 42_1-42_N) including several processing elements which are provided in one-to-one correspondence with several rows that make up least portion all the plurality of rows the photodetector array (Gowda; see Fig. 3; Col. 3, Ln. 53-67), each of the several processing elements performing predetermined parallel process on digital signals that are transferred from analog-to-digital converter array that equivalent to the signals outputted from the photodetectors in the corresponding row (Gowda; Col. 3, Ln. 13-21; Col. 7, Ln. 1-20; Gowda teaches the processing elements/ registers 42_1-42_N perform the double correlated sampling operation).

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda in view of Blessinger and further in view of Onishi (US-6,636,254).

With regarding to **claim 4,** Gowda in view of Blessinger fails to disclose a camera for high-speed image processing wherein the signal converter combines the output signal from the analog-to-digital converter array and the processed result signal, converts the combined signal into the image signal of the desired frame rate, and outputs the image signal. However, the limitations are well known in the art as taught by Onishi.

In the same field of endeavor, Onishi teaches an image processing apparatus wherein the signal converter / synthesizer (Fig. 10; 22) combines the raw images from endoscopes (Fig. 10; 2-2a) and the processed video signal, which is processed from the inverting circuit (Fig. 10; 11a-11b) (Col. 12, Ln. 61-67 – Col. 13, Ln. 1-3). Onishi further teaches that the synthesizing result produces a desired picture-in-picture image and selectively outputs to a TV monitor (Fig. 10; 21) (Col. 13, Ln. 4-13). In light of the teaching from Onishi, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the signal converter of Gowda and Blessinger by having the signal converter combines the output signal of the unprocessed video signal and the processed video signal taught by Onishi in order to provide a camera with a desired output capability such as picture-in-picture (Onishi; Col. 13, Ln. 1-5).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Yamane (US-5,875,004) discloses an image processing apparatus comprising a switch for selectively connecting the TV camera and a CPU to a display.

b) Shimamoto (US-6,147,712) discloses a format converter comprising a frame rate controller.

c) Etoh (US-6,118,483) discloses a high-speed image sensing apparatus.

d) Gowda (US-5,877,715) discloses an image sensor having a plurality of photo detectors arrays, A/D converters, and a double correlated sampling circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung H. Lam whose telephone number is 571-272-7320. The examiner can normally be reached on Monday - Friday 8AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's primary, NGOC YEN VU can be reached on 571-272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HL
08/05/2005

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